Design of a Double Tail Dynamic Comparator for Low Power and High Speed applications

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ABSTRACT

Now a days the entire world is running towards digitalization process in every field as digitalization is rapidly becoming one of the standard form of processing, storage and transmission of information. Digitalization is nothing but the conversion of traditional analog data into digital format in that scenario we necessitate a converter to change the analog data .so, in essential we go for ADC's.

The want of analog to digital converters with very-low power, area efficient and excessive speed is giving more chance to the use of dynamic regenerative comparators to increase the speed and power efficiency. Clocked comparators are regularly referred to as dynamic comparators. Dynamic double tail comparators are compared in terms of their power, speed and delay. The accuracy of comparators that is defined by using its electricity intake and speed is of eager interest in attaining over all better performance of ADCs. In the domain of signal processing with low power VLSI, the function of ADC device is crucial.

Many high speed ADCs, such as flash ADCs, require excessive speed, low power comparators with small chip area. Compared with the double tail comparator in the proposed comparator both the power consumption and delay time are substantially reduced. Design has particularly focused on delay of double-tail comparator, which are called clocked regenerative comparator. In this paper, an analysis on the delay of the dynamic comparators will be presented and analytical expressions are derived. From the analytical expressions, designers can obtain an intuition about the primary contributors to the comparator delay and fully explore the tradeoffs in dynamic comparator layout. Based on the existing analysis, a new dynamic comparator is proposed, where the circuit of traditional double tail dynamic comparator is altered for low power and fast operation even in small supply voltages. Here by adding a few transistors, the power consumptions can be reduced drastically. Post–layout simulation using 90nm CMOS technology confirms the analysis results of the proposed dynamic comparator.

Key Words: Analog to digital comparators, Clocked comparators, Dynamic double tail comparator, Flash ADC, Dynamic comparator.

1. INTRODUCTION

Comparator plays an important role in high speed analog to digital converters. A comparator is a device, which compares two analog signal or voltages and produce the digital output based on the comparison. Comparators are also referred to as 1-bit analog to digital converter, therefore they're regularly utilized in huge quantity in A/D converter. COMPARATOR is one of the foremost building blocks in most analog-to-digital converters (ADCs).Many high-speed ADCs, such as flash ADCs, require high-speed, low power comparators with small chip area. In design of ADCs, comparator of high speed, low power consumption are used.

Comparator in ultra-deep sub micrometer (UDSM) technologies suffers from low supply voltage. As a result design of

high velocity comparator is an assignment when the give voltage is low [1]. For this reason to obtain high pace in a given technology extra transistor are required and extra area and energy is required. Technique such as supply boosting method [2], [3] a technique such as body driven transistor [4], [5] has been developed to meet the low voltage design. In addressing switching problems and enter range two technique equivalent to boosting and bootstrapping are used. On this paper the prolong has been presented for quite a lot of dynamic comparator structure. The accuracy of such comparators, which is defined by its offset, along with power consumption, speed is of keen interest in achieving overall higher performance of ADCs. In the past, pre-amplifier based comparators have been used for ADC architectures such as flash and pipeline. The main drawback of pre-amplifier based comparators is the more offset voltage. To overcome this problem, dynamic comparators are often used that make a comparison once every clock period and require much less offset voltage. Nevertheless, these dynamic comparators suffer from giant power dissipation in comparison with pre-amplifier situated comparators. Apart from technological adjustments, setting up new circuit structures which preclude stacking too many transistors between the give rails is most efficient for low-voltage operation, especially if they do not develop the circuit complexity. Additional circuitry is added to the conventional dynamic comparator to enhance the comparator speed in low supply voltages.

In this paper, a comprehensive analysis about the delay of dynamic comparators has been presented for various architectures. Furthermore, based on the double-tail structure proposed in [6], a new dynamic comparator is presented, which does not require boosted voltage or stacking of too many transistors. Merely by adding a few minimum-size transistors to the conventional double-tail dynamic comparator, latch prolong time is profoundly diminished. This alteration also outcome in tremendous energy savings when in comparison with the conventional dynamic comparator and double-tail comparator. Situated on the double-tail architecture a new dynamic comparator has been awarded the place prolong is comparatively cut back compared to the prior design which doesn't require boosted voltage .By adding a few number of transistor the delay time at the latch has been comparatively reduce. As a result in the modified design the power is saved and can be used for high speed ADCs design.

The rest of this paper is organized as follows. Section II investigates the operation of the conventional clocked regenerative comparators and the pros and cons of each structure is discussed. Delay analysis is also presented and the analytical expressions for the delay of the comparators are derived. The proposed comparator is presented in Section III. Simulation results are addressed in Section IV, followed by conclusions in Section V.

II. CLOCK REGENERATIVE COMPARATORS

Clocked regenerative comparators have observed huge applications in many high-speed ADCs considering that they can make speedy decisions as a result of the strong optimistic feedback within the regenerative latch. The comparator is built with a dynamic CMOS latch [7]. Recently, many comprehensive analyses have been presented, which investigate the performance of these comparators from different aspects, such as noise [8], offset, random decision errors [9], and kick-back noise [10]. In this section, a comprehensive delay analysis is presented; the delay time of two common structures, i.e., conventional dynamic comparator and conventional dynamic double-tail comparator are analyzed, based on which the proposed comparator will be presented.

2.1. CONVENTIONAL DYNAMIC COMPARATOR

The conventional dynamic comparators have found wide applications in many high speeds ADC's since they can make fast decisions due to the strong positive feedback in the regenerative latch [11]. Many comprehensive analyses have been presented in recent years, which investigate the performance of comparator in different aspects. The operation

of the comparator is as follows. Start condition will happen when CLK=0(low), which leads to Mtail off and other transistor M7 & M8 makes both the output nodes Outp and Outn to V_{DD} [1]. When CLK=V_{DD} (high), transistor M7 and M8 ear off and Mtail is on. An output voltage which was pre- charged to high voltage, will start to discharge with different rates depending on the corresponding input voltage (INN/INP). Assuming the case where VINN>VINP Outn discharges faster than Outp, hence when Outn (discharged by transistor M1 drain current), falls down to V_{DD} - $|V_{thn}|$ before Outp. (Discharged by transistor M2 drain current) the corresponding pMOS transistor (M6) will turn on initiating latch regeneration by inverters (M3, M5 and M4, M6). Thus, Outp pulls to V_{DD} and Outn discharges to ground. If VINN < VINP, the circuit works vice versa.

The delay of the above comparator consists of two delay t_0 and t_{latch} where to discharging delay of the load capacitance

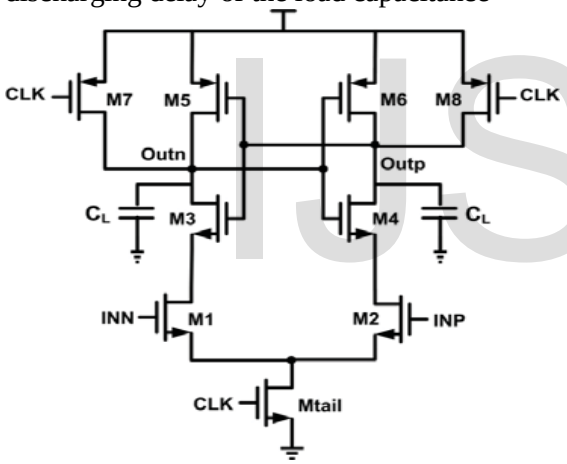


Fig2.1.Schematic diagram of conventional dynamic comparator

C_L and t_{latch} is the latching delay of the cross coupled inverter and hence the total delay (t_{delay}) of the above comparator is given as

$$t_{delay} = t_0 + t_{latch}$$
$$= 2\frac{C_L|V_{thp}|}{I_{tail}} + \frac{C_L}{g_{m,eff}} \cdot \ln\left(\frac{V_{DD}}{4|V_{thp}|\Delta V_{in}}\sqrt{\frac{I_{tail}}{\beta_{1,2}}}\right).$$

Where C_L is the load capacitance, $|V_{thp}|$ is the threshold voltage of M2 transistor, $g_{m,eff}$ is the transconductance of the back-to-back inverter, V_{DD} is the supply voltage, I tail is the current of the Mtail transistor. $\beta_{1,2}$ is the current factor of the input transistor, ΔV_{in} is the input voltage difference. According to equation (1) the delay of the above comparator depends directly to the load capacitance (C_L) and inversely to input difference voltage (ΔV_{in}).

In principle, this structure has the advantages of high input impedance, rail-to-rail output swing, no static power consumption, and good robustness against noise and mismatch [1]. Due to the fact that parasitic capacitances of input transistors do not directly affect the switching speed of the output nodes, it is possible to design large input transistors to minimize the offset. The disadvantage, on the other hand, is the fact that due to several stacked transistors, a sufficiently high supply voltage is needed for a proper delay time. The reason is that, at the beginning of the decision, only transistors *M*3 and *M*4 of the latch contribute to the positive feedback until the voltage level of one output node has dropped below a level small enough to turn on transistors *M*5 or *M*6 to start complete regeneration. At a low supply voltage, this voltage drop only contributes a small gate-source voltage for transistors *M*3 and *M*4, where the gate source voltage of *M*5 and *M*6 is also small; thus, the delay time of the latch becomes large due to lower transconductance. Another important drawback of this structure is that there is only one current path, via tail transistor M_{tail}, which defines the current for both the differential amplifier and the latch (the cross-coupled inverters). While one would like a small tail current to keep the differential pair in weak inversion and obtain a long integration interval and a better G_m/I ratio, a large tail current would be desirable to enable fast regeneration in the latch [12]. Besides, as far as M_{tail} operates mostly in triode region, the tail current depends on input common-mode voltage, which is not favorable for regeneration.

2.2. CONVENTIONAL DOUBLE TAIL COMPARATOR

A conventional double-tail comparator is shown in Fig. 3 [11]. This topology has less stacking and therefore can operate at lower supply voltages compared to the conventional dynamic comparator. The double tail enables both a large current in the latching stage and

wider M_{tail2}, for fast latching independent of the input common-mode voltage (V_{cm}), and a small current in the input stage (small M_{tail1}), for low offset [10].

The operation of this comparator is as follows (see Fig. 4). During reset phase (CLK = 0, M_{tail1}, and M_{tail2} are off), transistors $M3$-$M4$ pre-charge fn and fp nodes to V_{DD}, which in turn causes transistors M_{R1} and M_{R2} to discharge the output nodes to ground. During decision-making phase (CLK =V_{DD}, M_{tail1} and Mtail2 turn on), $M3$-$M4$ turn off and voltages at nodes fn and fp start to drop with the rate defined by $I_{Mtail1}/C_{fn(p)}$ and on top of this, an input-dependent differential voltage $\Delta V_{fn(p)}$ will build up. The intermediate stage formed by M_{R1} and M_{R2} passes $\Delta V_{fn(p)}$ to the cross coupled inverters and also provides a good shielding between input and output, resulting in reduced value of kickback noise [8].

Similar to the conventional dynamic comparator, the delay of this comparator comprises two main parts, t_0 and t_{latch}. The delay

t_0 represents the capacitive charging of the load capacitance C_{Lout} (at the latch stage output nodes, Out$n$ and Out$p$) until the first n-channel

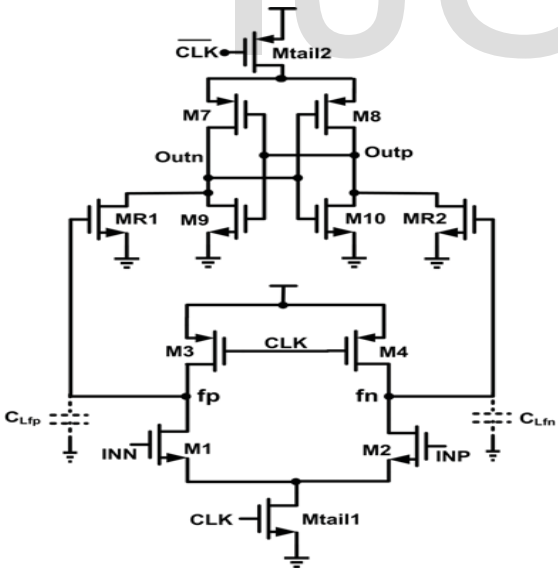


Fig2.2.Schematic diagram of the conventional double tail dynamic comparator

transistor ($M9$/$M10$) turns on, after which the latch regeneration starts; thus t_0 is obtained where I_{B1} is the drain current of the $M9$ (assuming VINP >VINN, see Fig. 3) and is approximately equal to the half of the tail current (I_{tail2}).

After the first n-channel transistor of the latch turns on (for instance, $M9$), the corresponding output (e.g., Out$n$) will be discharged to the ground, leading front p-channel transistor (e.g., $M8$) to turn on, charging another output (Out$p$) to the supply voltage (V_{DD}).

The differential voltage at nodes fn/fp ($\Delta V_{fn/fp}$) at time t_0 can be achieved from

$$\begin{aligned}\Delta V_{fn/fp} &= \left|V_{fn}(t=t_0) - V_{fp}(t=t_0)\right| \\ &= t_0 \cdot \frac{I_{N1} - I_{N2}}{C_{L,fn(p)}} \\ &= t_0 \cdot \frac{g_{m1,2}\Delta V_{in}}{C_{L,fn(p)}}.\end{aligned}$$

In this equation, I_{N1} and I_{N2} refer to the discharging currents of input transistors ($M1$ and $M2$), which are dependent on the input differential voltage (i.e., $\Delta I_N = g_{m1,2}\Delta V_{in}$).

This equation shows that $\Delta V0$ depends strongly on the transconductance of input and intermediate stage transistors, input voltage difference (ΔVin), latch tail current, and the capacitive ratio of C_{Lout} to $C_{L,fn(p)}$.

$$\begin{aligned}\Delta V_0 &= 2V_{Thn}\frac{g_{mR1,2}}{I_{tail2}}\Delta V_{fn/fp} \\ &= \left(\frac{2V_{Thn}}{I_{tail2}}\right)^2 \cdot \frac{C_{Lout}}{C_{L,fn(p)}} \cdot g_{mR1,2}g_{m1,2}\Delta V_{in}.\end{aligned}$$

Substituting $\Delta V0$ in latch regeneration time, the total delay of this comparator is achieved as follows:

$$\begin{aligned}t_{delay} &= t_0 + t_{latch} = 2\frac{V_{Thn}C_{Lout}}{I_{tail2}} + \frac{C_{Lout}}{g_{m,eff}} \cdot \ln\left(\frac{V_{DD}/2}{\Delta V_0}\right) \\ &= 2\frac{V_{Thn}C_{Lout}}{I_{tail2}} + \frac{C_{Lout}}{g_{m,eff}} \\ &\quad \cdot \ln\left(\frac{V_{DD} \cdot I_{tail2}^2 \cdot C_{L,fn(p)}}{8V_{Thn}^2 \cdot C_{Lout}g_{mR1,2}g_{m1,2}\Delta V_{in}}\right).\end{aligned}$$

From the equations derived for the delay of the double-tail comparator, some important notes can be concluded.

1) The voltage difference at the first stage outputs ($\Delta V_{fn/fp}$) at time t_0 has a profound effect on latch preliminary differential output voltage (ΔV_0) and consequently on the latch delay. As a consequence, increasing it would

profoundly diminish the delay of the comparator.

2) In this comparator, both intermediate stage transistors will be finally cut-off, (since fn and fp nodes both discharge to the ground), accordingly they do not play any role in improving the effective transconductance of the slatch. Besides, during reset phase, these nodes have to be charged from ground to V_{DD}, which means power consumption. The following section describes how the proposed comparator improves the performance of the double-tail comparator from the above points of view.

III.PROPOSED DOUBLE-TAIL DYNAMIC COMPARATOR

Fig. 3 demonstrates the schematic diagram of the double tail comparator. Double tail architecture has two tail transistors. Double tail comparator is used for low power applications. In this technique, increase the voltage difference between the output nodes in order to increase the latch regeneration speed. For this purpose, two control transistors have been added to the first stage in parallel to M3 and M4 transistors but in a cross-coupled manner. Double tail comparator has two operation modes, the reset phase and the decision making phase. The modes of operation depend on the clock input given. CLK = 0 known as reset phase and CLK = V_{DD} known as evaluation phase. When CLK = 0, nMos transistor is in off and pMos transistor is in on. When CLK = V_{DD}, nMOS is in on and pMOS transistor is in off.

The operation of the proposed comparator is as follows. When CLK = 0, the reset phase, both the tail transistors Mtail1 and Mtail2 are in off to avoiding static power. Transistor M3 and M4 are in on. M3 and M4 pulls both fn and fp nodes to V_{DD}, as a consequence transistor MC1 and MC2 are cut off. The circuit has two intermediate stage transistors MR1 and MR2. These transistors reset both latch outputs to ground.

During decision-making phase, CLK = V_{DD}, both the tail transistors are on, M3 and M4 transistors are off. At the beginning of this phase, the control transistors MC1 and Mc2 are still off (since fn and fp are about V_{DD}). Thus, fn and fp start to drop with different rates according to the input voltages. Suppose

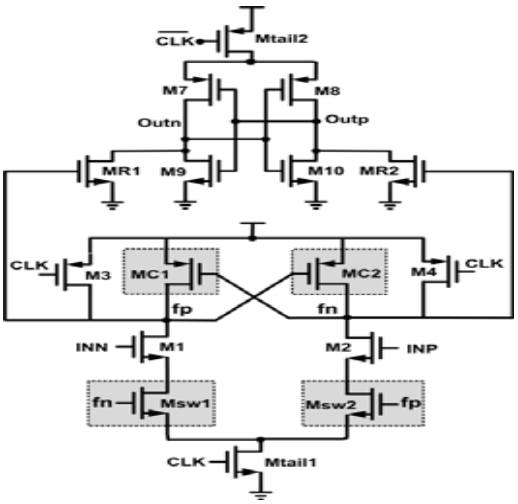
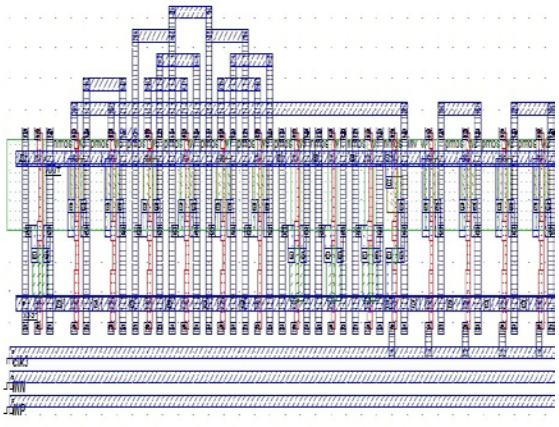


Fig 3.Schematic diagram of the proposed double tail dynamic comparator

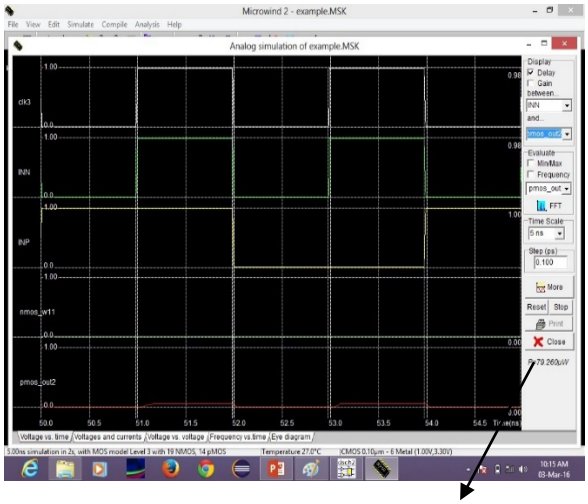
VINP > VINN, thus fn drops faster than fp, (since M2 provides more current than M1). As long as fn continues falling, the corresponding pMOS control transistor (MC1 in this case) starts to turn on, pulling fp node back to the V_{DD}, so another control transistor remains off, allowing fn to be discharged completely.

When one of the control transistors turns on, a current from V_{DD} is drawn to the ground via input and tail transistor (ie, MC1, M1, and Mtail1) result in static power consumption. To overcome this limitation, two nMOS switches are used below the input transistors such asM_{sw1} and M_{sw2}. At the beginning of the decision making phase, due to the fact that both fn and fp nodes have been pre-charged to V_{DD} (during the reset phase), both switches are closed and fn and fp start to drop with different discharging rates. As soon as the comparator detects that one of the fn or fp nodes is discharging faster, control transistors will act in a way to increase their voltage difference. Suppose that fp is pulling up to the V_{DD} and fn should be discharged completely, hence the switch in the charging path of fp will be opened, but the other switch connected to fn will be closed to allow the complete discharge of fn node. In other words, the operation of the control transistors with the switches emulates the operation of the latch.

IV.STIMULATION RESULTS



(a) Layout of proposed double tail dynamic comparator in 90nm Cmos technology

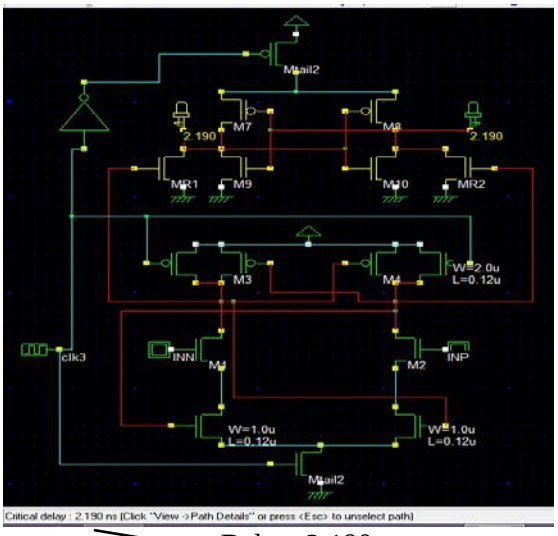


Power=79.260µW

C) Power output of proposed double tail dynamic comparator in 90nm Cmos technology

TABLE: PERFORMANCE COMPARISON

Comparator structure	Dynamic Comparator	Conventional double tail dynamic comparator	Proposed double tail dynamic comparator
Technology CMOS	90nm	90nm	90nm
Supply voltage(V)	1.2	1.2	1.2
Delay(ns)	2.35	2.21	2.190
Power(µW)	6.143	89.751	79.260



Delay=2.190ns

(b) Delay output of proposed double tail dynamic comparator in 90nm Cmos technology

V.CONCLUSION

In this paper, we presented a comprehensive delay analysis for clocked dynamic comparators and expressions were derived. Two common structures of conventional dynamic comparator and conventional double-tail dynamic comparators were analyzed. Also, based on theoretical analyses, a new dynamic comparator with low-delay low-power capability was proposed in order to improve the performance of the comparator. A new proposed double-tail comparator shows better performance as compared to conventional dynamic and double-tail dynamic comparator. The proposed double-tail dynamic comparator can be used for the design of high speed ADCs as the delay is reduced and hence the operation will be faster.

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